Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **OFFSET N1**
2. **IN-**
3. **IN+**
4. **VCC-**
5. **OFFSET N2**
6. **OUT**
7. **VCC+**

**.056”**

**.045”**

**2**

**1**

**3**

**4**

**5**

**6 7**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref: None**

**APPROVED BY: DK DIE SIZE .045” X .056” DATE: 4/27/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .010” P/N: TL081**

**DG 10.1.2**

#### Rev B, 7/19/02